(c) disconnecting said test circuit from respective voltage terminals providing said first and second voltage levels; and

(d) measuring said parameter of said circuit under test with said test circuit.

3. (Amended) The method of claim 1, wherein said act of charging a first portion comprises charging a first capacitor of said test circuit to a power rail voltage level, and wherein said act of charging a second portion comprises charging a second capacitor of said test circuit to a predetermined reference voltage level.

6. (Amended) The method of claim 3 further comprising:

changing said predetermined reference voltage level; and

repeating acts (a) through (d) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

8. (Amended) The method of claim 6, wherein said act of repeating comprises repeating acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

9. (Amended) The method of claim 8, wherein said act of repeating comprises repeating acts (a) through (d) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

10. (Amended) The method of claim 6, wherein said act of repeating comprises repeating acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

A3

11. (Amended) The method of claim 10, wherein said act of repeating comprises repeating acts (a) through (d) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.

A4

24. (Amended) A test circuit for measuring a parameter of a circuit under test, said test circuit comprising:

a first charging portion for charging a first portion of said test circuit to a first voltage level;

a second charging portion for charging a second portion of said test circuit to a second voltage level;

respective switches within said first and second charging portions for disconnecting said test circuit from terminals respectively providing said first and second voltage levels; and

a measuring portion for measuring a parameter of said circuit under test while said test circuit is disconnected from said terminals.

25. (Amended) The test circuit of claim 24, wherein said first charging portion comprises a first storage capacitor for storing a charge of said first voltage level.

26. (Amended) The test circuit of claim 25, wherein said switch within said first charging portion comprises a first transistor, a first side of said first transistor being coupled to said first storage capacitor, a second side of said first transistor being coupled to said terminal providing said first voltage level.

27. (Amended) The test circuit of claim 24, wherein said measuring portion comprises a comparator.

A5

31. (Amended) The test circuit of claim 28, wherein a second input of said comparator is coupled to said terminal providing said second voltage level, said terminal being a reference voltage terminal for providing a reference voltage, said comparator comparing said reference voltage with said sensed parameter of said circuit under test.

32. (Amended) The test circuit of claim 31 wherein said switch within said second charging portion comprises a switch coupled between said second input of said comparator and said reference voltage terminal for disconnecting said second input of said comparator from said reference voltage terminal.

33. (Amended) The test circuit of claim 32, wherein said switch within said second charging portion comprises a transistor.

35. (Amended) The test circuit of claim 32, wherein said second charging portion comprises a second storage capacitor for providing said reference voltage to said second input of said comparator when said second input is disconnected from said reference voltage terminal.

A4

38. (Amended) A semiconductor die comprising:

at least one circuit to be tested; and

at least one test circuit for measuring a parameter of said at least one circuit to be tested, said at least one test circuit comprising:

a first charging portion for charging a first portion of said at least one test circuit to a first voltage level;

a second charging portion for charging a second portion of said at least one test circuit to a second voltage level;

A4

respective switches within said first and second charging portions for disconnecting said at least one test circuit from terminals respectively providing said first and second voltage levels; and

a measuring portion for measuring said parameter of said at least one circuit to be tested while said at least one test circuit is disconnected from said terminals.

39. (Amended) The die of claim 38, wherein said first charging portion comprises a first storage capacitor for storing a charge of said first voltage level.

40. (Amended) The die of claim 39, wherein said switch within said first charging portion comprises a first transistor, a first terminal of said first transistor being coupled to said first storage capacitor, a second terminal of said first transistor being coupled to said terminal providing said first voltage level.

41. (Amended) The die of claim 38, wherein said measuring portion comprises a comparator.

A7

45. (Amended) The die of claim 42, wherein a second input of said comparator is coupled to said terminal providing said second voltage level, said terminal being a reference voltage terminal for providing a reference voltage, said comparator comparing said reference voltage with said sensed parameter of said at least one circuit to be tested.

46. (Amended) The die of claim 45 wherein said switch within said second charging portion comprises a switch coupled between said second input of said comparator and said reference voltage terminal for disconnecting said second input of said comparator from said reference voltage terminal.

47. (Amended) The die of claim 46, wherein said switch within said second charging portion comprises a transistor.

A7

49. (Amended) The die of claim 46, wherein said second charging portion comprises a second storage capacitor for providing said reference voltage to said second input when said second input is disconnected from said reference voltage terminal.

A8

51. (Amended) A semiconductor die comprising:

at least one circuit to be tested; and

at least one test circuit for measuring a parameter of said at least one circuit to be tested, said at least one test circuit comprising:

a comparator coupled to a power source, said comparator having a first input for receiving a sensed voltage and a second input for receiving a reference voltage;

a first storage capacitor coupled to said power source and also coupled to said comparator, said first storage capacitor being used for storing a voltage supplied by said power source and also for providing power to said comparator when said comparator is disconnected from said power source;

a second storage capacitor coupled to a reference voltage source and also coupled to said second input of said comparator, said second storage capacitor being used for storing a reference voltage provided by said reference voltage source and also for providing said second input of said comparator with said reference voltage when said comparator is disconnected from said reference voltage source.

A9

53. (Amended) A computer readable storage medium storing a computer readable program for measuring a parameter of a circuit under test, said computer readable program being configured to operate a computer to:

(a) charge a first portion of a test circuit up to a first voltage level;

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(b) charge a second portion of said test circuit up to a second voltage level;

(c) disconnect said test circuit from respective voltage terminals providing said first and second voltage levels; and

(d) measure said parameter of said circuit under test with said test circuit.

55. (Amended) The storage medium of claim 53, wherein said program is further configured to operate said computer to charge a first capacitor of said test circuit to a power rail voltage level, and also to charge a second portion comprises charging a second capacitor of said test circuit to a predetermined reference voltage level.

A10

58. (Amended) The storage medium of claim 55, wherein said program is further configured to operate said computer to:

change said predetermined reference voltage level; and

repeat acts (a) through (d) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

A11

60. (Amended) The storage medium of claim 58, wherein said program is further configured to operate said computer to repeat acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

61. (Amended) The storage medium of claim 60, wherein said program is further configured to operate said computer to repeat acts (a) through (d) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

62. (Amended) The storage medium of claim 58, wherein said program is further configured to operate said computer to repeat acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

A11

63. (Amended) The storage medium of claim 62, wherein said program is further configured to operate said computer to repeat acts (a) through (d) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.

A12

76. (Amended) A processor system, comprising:

a processor; and

a communications link coupled to said processor and also coupled to a computer readable storage medium, wherein

said computer readable storage medium stores a computer program for measuring a parameter of a circuit under test, said computer program configured to operate said processor to:

(a) charge a first portion of a test circuit up to a first voltage level;

(b) charge a second portion of said test circuit up to a second voltage level;

(c) disconnect said test circuit from respective voltage terminals providing said first and second voltage levels; and

(d) measure said parameter of said circuit under test with said test circuit.

78. (Amended) The processor system of claim 76, wherein said program is further configured to operate said processor to charge a first capacitor of said test circuit to a power rail voltage level, and also to charge a second capacitor of said test circuit to a predetermined reference voltage level.

A13

81. (Amended) The processor system of claim 78, wherein said program is further configured to operate said processor to:

change said predetermined reference voltage level; and

repeat acts (a) through (d) if said measured parameter does not have a predetermined relationship with said predetermined reference voltage level.

A14

83. (Amended) The processor system of claim 81, wherein said program is further configured to operate said processor to repeat acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

84. (Amended) The processor system of claim 83, wherein said program is further configured to operate said processor to repeat acts (a) through (d) if a voltage measured at a ground terminal is not less than said predetermined reference voltage level.

85. (Amended) The processor system of claim 81, wherein said program is further configured to operate said processor to repeat acts (a) through (d) if a measured voltage is not less than said predetermined reference voltage level.

86. (Amended) The processor system of claim 85, wherein said program is further configured to operate said processor to repeat acts (a) through (d) if a voltage measured at a power rail of said circuit under test is not less than said predetermined reference voltage level.